

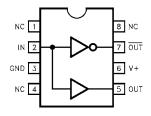
Data Sheet June 15, 2006 FN7281.1

2-Phase, High Speed CCD Driver

The EL7182 is extremely well suited for driving CCD's, especially where high contrast imaging is desirable. The 16V supply rating is attractive for higher voltage CCD applications, as in color fax machines. The input is TTL and 3V compatible. The low quiescent current requirement is advantageous in portable/battery powered systems. The EL7182 is available in 8 Ld PDIP and 8 Ld SOIC packages.

Pinout

EL7182 (8 LD PDIP, SOIC) TOP VIEW



Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Features

- · 3V and 5V Input compatible
- · Clocking speeds up to 10MHz
- · Reduced clock skew
- · 20ns Switching/delay time
- · 2A Peak drive
- · Low quiescent current
- Wide operating voltage: 4.5V-16V
- Pb-free plus anneal available (RoHS compliant)

Applications

- · CCD Drivers requiring high-contrast imaging
- · Differential line drivers
- · Push-pull circuits

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #		
EL7182CN	EL7182CN	-40 to +85	8 Ld PDIP	MDP0031		
EL7182CS	7182CS	-40 to +85	8 Ld SOIC	MDP0027		
EL7182CSZ (Note)	7182CSZ	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027		
EL7182CSZ-T7 (Note)	7182CSZ	8 Ld SOIC (7" Tape and Reel) (Pb-free)				
EL7182CSZ-T13 (Note)	7182CSZ	8 Ld SOIC (7 (Pb-free)	" Tape and R	eel)		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply (V+ to Gnd)		Operating Junction Temperature	125°C
Input Pins	0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current		SOIC	
Storage Temperature Range	65°C to +150°C	PDIP	
Ambient Operating Temperature	40°C to +85°C		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $T_A = 25$ °C, V = 15V unless otherwise specified

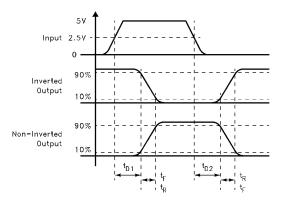
PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT		-	'		"	
V _{IH}	Logic "1" Input Voltage		2.4			V
I _{IH}	Logic "1" Input Current	@V+		0.1	10	μA
V _{IL}	Logic "0" Input Voltage				0.8	V
I _{IL}	Logic "0" Input Current	@0V		0.1	10	μA
V _{HVS}	Input Hysteresis			0.3		V
OUTPUT			<u> </u>			
R _{OH}	Pull-Up Resistance	I _{OUT} = -100mA		3	6	Ω
R _{OL}	Pull-Down Resistance	I _{OUT} = +100mA		4	6	Ω
I _{PK}	Peak Output Current	Source		2		Α
		Sink		2		Α
I _{DC}	Continuous Output Current	Source/Sink	100			mA
POWER SUPPL	Υ	'		1		1
Is	Power Supply Current	Input High		2.5	5	mA
Vs	Operating Voltage		4.5		16	V

AC Electrical Specifications $T_A = 25$ °C, V = 15V unless otherwise specified

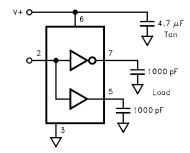
PARAMETER	DESCRIPTION	SCRIPTION TEST CONDITIONS MIN		TYP	MAX	UNITS		
SWITCHING CHARACTERISTICS								
t _R	Rise Time	C _L = 500pF		7.5		ns		
		C _L = 1000pF		10	20	ns		
t _F	Fall Time	C _L = 500pF		10		ns		
		C _L = 1000pF		13	20	ns		
t _{D-ON}	Turn-On Delay Time			18	25	ns		
t _{D-OFF}	Turn-Off Delay Time			20	25	ns		

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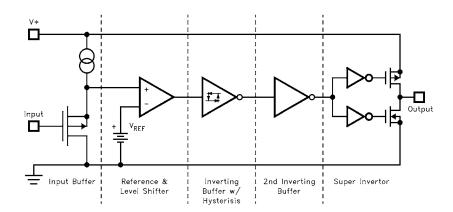
Timing Table



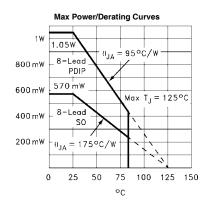
Standard Test Configuration

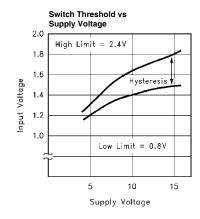


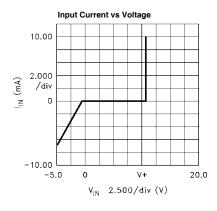
Simplified Schematic

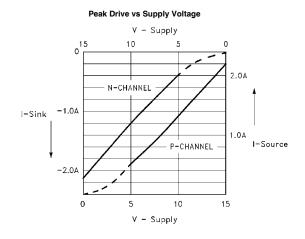


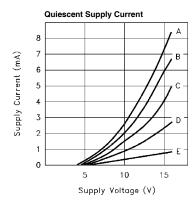
Typical Performance Curves

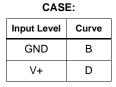


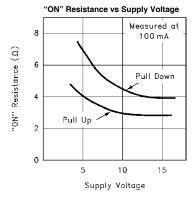


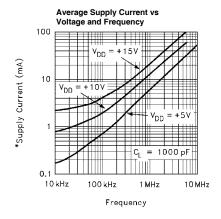


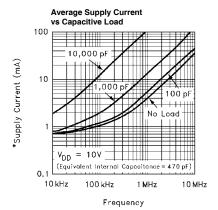




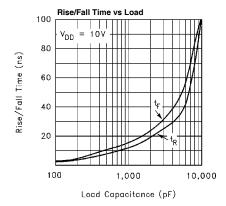


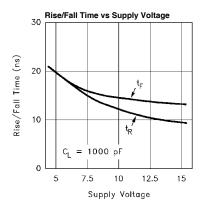


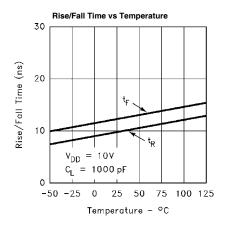


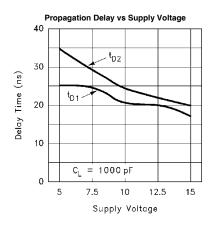


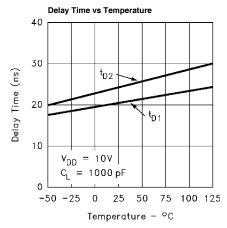
Typical Performance Curves (Continued)





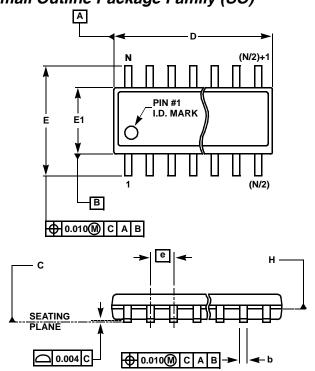


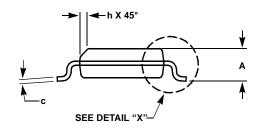


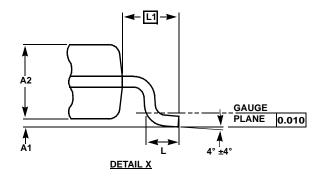


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Small Outline Package Family (SO)







MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

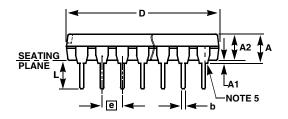
			SO16	SO16 (0.300")	SO20	SO24	SO28		
SYMBOL	SO-8	SO-14	(0.150")	(SOL-16)	(SOL-20)	(SOL-24)	(SOL-28)	TOLERANCE	NOTES
Α	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
С	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
Е	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
е	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

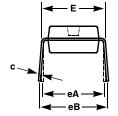
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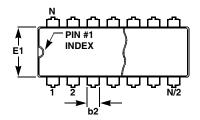
NOTES:

- 1. Plastic or metal protrusions of 0.006" maximum per side are not included.
- 2. Plastic interlead protrusions of 0.010" maximum per side are not included.
- 3. Dimensions "D" and "E1" are measured at Datum Plane "H".
- 4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)







MDP0031 PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	TOLERANCE	NOTES
Α	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
С	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
е	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. B 2/99

NOTES:

- 1. Plastic or metal protrusions of 0.010" maximum per side are not included.
- 2. Plastic interlead protrusions of 0.010" maximum per side are not included.
- 3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
- 4. Dimension eB is measured with the lead tips unconstrained.
- 5. 8 and 16 lead packages have half end-leads as shown.

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